What is claimed is:

1. A multi-bit phase shifter comprises:

one or more phase shifters each including a short stub with an end short; and

an MEMS (Micro Electro Mechanical System) switch formed at the short stub and controlling an impedance value.

2. The multi-bit phase shifter of claim 1 further comprising:

an open stub connected to the short stub in parallel to obtain a wider bandwidth and smoothing phase characteristics; and

a DC bias line for lowering a driving voltage of the MEMS switch.

3. The multi-bit phase shifter of claim 1 further comprising:

an air gap coupler for maintaining a stable phase difference on a line.

4. The multi-bit phase shifter of claim 1, wherein the phase shifter generates a phase difference by a multiple of 11.25°.

5. The multi-bit phase shifter of claim 1, wherein the phase shifter is 11.25°/22.5°/45°/180°/90° phase shifters.

6. The multi-bit phase shifter of claim 5, wherein the 11.25°/22.5°/45° phase shifters include a stub with an end short, instead of an inductor or a capacitor, and loads the MEMS switch at the end of the stub to use a phase

difference of a reflected wave according to a capacitor on-off ratio.

7. The multi-bit phase shifter of claim 5, wherein the 180°/90° phase shifters are reflection type phase shifters using a coupler.

8. The multi-bit phase shifter of claim 5 further comprising:

an air bridge for forming a common ground among grounds of the phase shifters.

9. A multi-bit phase shifter comprising:

a first phase shifter including a short stub with an end short, an open stub for smoothing phase characteristics, an MEMS (Micro Electro Mechanical System) switch formed at the end of the short stub and controlling an impedance value, and a DC bias line for lowering a driving voltage of the MEMS switch; and

a second phase shifter including a short stub with an end short, an MEMS switch formed at the end of the short stub and controlling an impedance value, and a DC bias line for lowering a driving voltage of the MEMS switch.

10. The multi-bit phase shifter of claim 9, wherein, as for the first phase shifter, one or more first phase shifters are connected to generate a phase difference by a multiple of 11.25°.

11. The multi-bit phase shifter of claim 9, wherein the second phase shifter generates a phase difference by a multiple of 90° by controlling the MEMS switches.

12. The multi-bit phase shifter of claim 9, wherein the second phase shifter further includes an air gap coupler for maintaining a stable phase difference among the short stubs.

13. The multi-bit phase shifter of claim 9, wherein the open stub is connected in parallel to the short stub in order to secure a wide bandwidth.

14. The multi-bit phase shifter of claim 9 further comprising:

an air bridge for forming a common ground between grounds of the first phase shifter and the second phase shifter.

15. The multi-bit phase shifter of claim 9, wherein the phase shifter includes a 5-bit phase shifter including a 11.25° phase shifter having one first phase shifter, a 22.5° phase shifter having two first phase shifters, a 45° phase shifter having two first phase shifters, a 90° phase shifter having the second phase shifter, and a 180° phase shifter having the second phase shifter.

16. A method for manufacturing a multi-bit phase shifter comprising:

a first step of forming a first conductive film pattern making a signal line on a substrate, an insulation film pattern on the first conductive film pattern, and forming a resistor pattern along a DC bias line;

a second step of sequentially forming a first photoresist pattern, a seed layer and a second photoresist pattern on the resulting structure, and forming an electrode through the seed layer;

a third step of removing the second photoresist pattern, etching a portion

of the seed layer to form a switch pattern, and removing the remaining portion; and

a fourth step of forming a third photoresist pattern on the resulting structure, forming a conductive film stacking pattern on the third photoresist pattern to form an air bridge and an air coupler, and removing the photoresist.

17. The method of claim 16, wherein, in the first step, Cr/Pt is formed on the substrate and patterned to form a first conductive film pattern making the signal line and an AlN insulation film pattern is formed on the first conductive film pattern, on which TaN or Nichrome is formed and a resistor pattern is formed along the DC bias line.

18. The method of claim 16, wherein, in the second step, the first photoresist pattern is formed to form a basic molding for formation of an electrode, on which Au/Cr seed layer is formed, on which the second photoresist pattern the same as the first photoresist pattern is formed to form a photoresist molding for formation of an electrode, and Au electrode is formed by using the molding structure and the seed layer.

19. The method of claim 16, wherein, in the third step, after the second photoresist pattern (PR2) is removed, a chrome mask (MK) is applied and a portion of the seed layer is formed in a hinge pattern of the MEMS switch.

20. The method of claim 16, wherein, in the fourth step, in forming the third photoresist pattern, portions of each electrode to which the air bridge and the

air coupler are connected are exposed, the second conductive film and the third conductive film are sequentially formed on the resulting structure, a patterning is formed according to the structure of the air bridge and the air coupler, and then, the first photoresist pattern and the third photoresist pattern formed in the structure are all removed.